

ARMY RESEARCH LABORATORY



A High-Temperature Printed Circuit Board

by Bruce R. Geil and Merle W. DeLancey

ARL-MR-339

November 1996

The findings in this report are not to be construed as an official Department of the Army position unless so designated by other authorized documents.

Citation of manufacturer's or trade names does not constitute an official endorsement or approval of the use thereof.

Destroy this report when it is no longer needed. Do not return it to the originator.

Army Research Laboratory

Adelphi, MD 20783-1197

ARL-MR-339

November 1996

A High-Temperature Printed Circuit Board

Bruce R. Geil and Merle W. DeLancey

Sensors and Electron Devices Directorate

sponsored by

Space and Strategic Defense Command

PO Box 1500

Huntsville, AL 35807-3801

Abstract

Working with the U.S. Army Space and Strategic Defense Command, the Army Research Laboratory has developed an easy-to-produce, reliable, high-temperature printed circuit board for radiation studies of circuits that use silicon carbide transistors. This board is designed to operate at temperatures beyond 300°C. The board consists of an alumina substrate with thick-film gold traces. Stainless-steel pin receptacles are used to mount the transistors, allowing easy insertion and removal. Ruthenium oxide resistors are glued to the substrate and wire-bonded for electrical connection.

Contents

1. Introduction	1
2. Operational Amplifier PCB Development	2
3. Conclusion	8
Acknowledgments	9
References	9
Distribution	11
Report Documentation Page	15

Figures

1. Board overview	1
2. Pin receptacle design	2
3. Board schematic	3
4. Mask layout	3
5. Board after gold patterning	5
6. Closeup of resistor and pin receptacle mounts	7
7. Closeup of resistor mounting.....	8

Tables

1. Chemical solutions used in PCB fabrication	4
2. Aremco high-temperature ceramic adhesive properties	7

1. Introduction

Recent developments in high-temperature semiconductors such as 6H-SiC have created discrete transistors that can operate at temperatures exceeding 300°C and at high levels of radiation. The Army Research Laboratory (ARL) has been working on a project for the U.S. Army Space and Strategic Defense Command (USA SSDC) to develop a radiation-hardened high-temperature amplifier circuit. The amplifier circuit is a two-stage differential amplifier that uses 6H-silicon carbide (SiC) junction field-effect transistors (JFETs) as the active devices [1,2]. This new high-temperature technology will allow electronics to be used in applications that presently require remote sensors and controls. Some of these include internal combustion engine controls, jet engine exhaust monitoring, and nuclear power applications.

The transistors are individually packaged in TO-46 headers, and hermetically sealed to prevent electrode oxidation at high-temperatures. These devices, along with other components, were required to be integrated into a small package, so that the resulting circuits would fit into the radiation test equipment. To this end, a high-temperature printed circuit board (PCB) was devised (see fig. 1). This PCB allows the discrete components, transistors, capacitors, and resistors to be wired together to produce small-area circuits.

The PCB, fabricated at ARL's Semiconductor Engineering and Materials (SEMT) facility, followed some of the techniques developed by other groups [3,4], with changes made to accommodate readily available processing techniques. This allowed rapid turnaround as needs were identified. All the techniques used in fabricating this board can be easily transferred into mass production. The PCB must withstand 300°C and be able to fit into the radiation test chamber. The PCB allows for replacement of transistors and easy testing of each circuit node at the bench.

Figure 1. Board overview.



2. Operational Amplifier PCB Development

Alumina was selected for the substrate since it is compatible with thick-film conductor pastes, can handle high temperatures (above 1000°C), and is strong enough for repeated transistor-insert cycles. To allow plug-in mounting of the packaged transistors, pin receptacles [5] from Advanced Interconnections (fig. 2) were used. The receptacles are nickel-coated stainless steel with a nickel/beryllium spring inside to allow positive contact to the transistor pins. These pin receptacles, unlike other pin receptacles, can handle the high temperatures encountered by the board. A gold-based thick-film paste, Dupont 5715, was chosen as the conducting material, since it allows use of readily available integrated circuit techniques to pattern the PCB traces. Typically, thick-film patterns are applied through a metal screen mask. Since it would require several weeks to obtain a patterned screen, the gold was applied through a blank screen, and then etched with a photopatternable mask and an iodine-based gold etch. This technique is used extensively in the production of integrated circuits. Because these standard methods were used, only one week was required for fabrication of these PCBs.

Figure 3 shows the electrical schematic, and figure 4 shows the PCB layout that was produced at the ARL SEMT facility via standard integrated circuit masking techniques. Originally, the design rules for the PCB layout specified a 1-mil line width. After one of the alumina substrates was patterned with an iodine-based gold etch (table 1), it was found that undercutting of the photoresist caused electrical shorts in the gold lines. As a remedy for this problem, the line widths were increased to 5 mils.

Figure 2. Pin receptacle design.

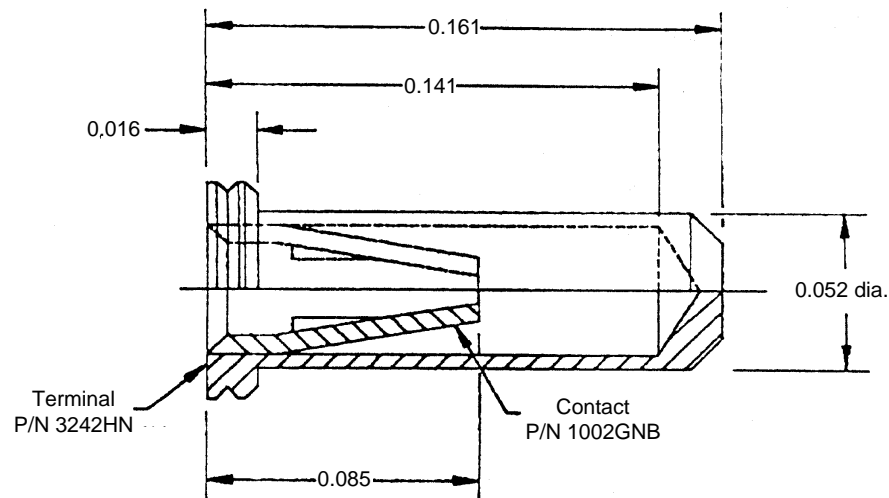


Figure 3. Board schematic.

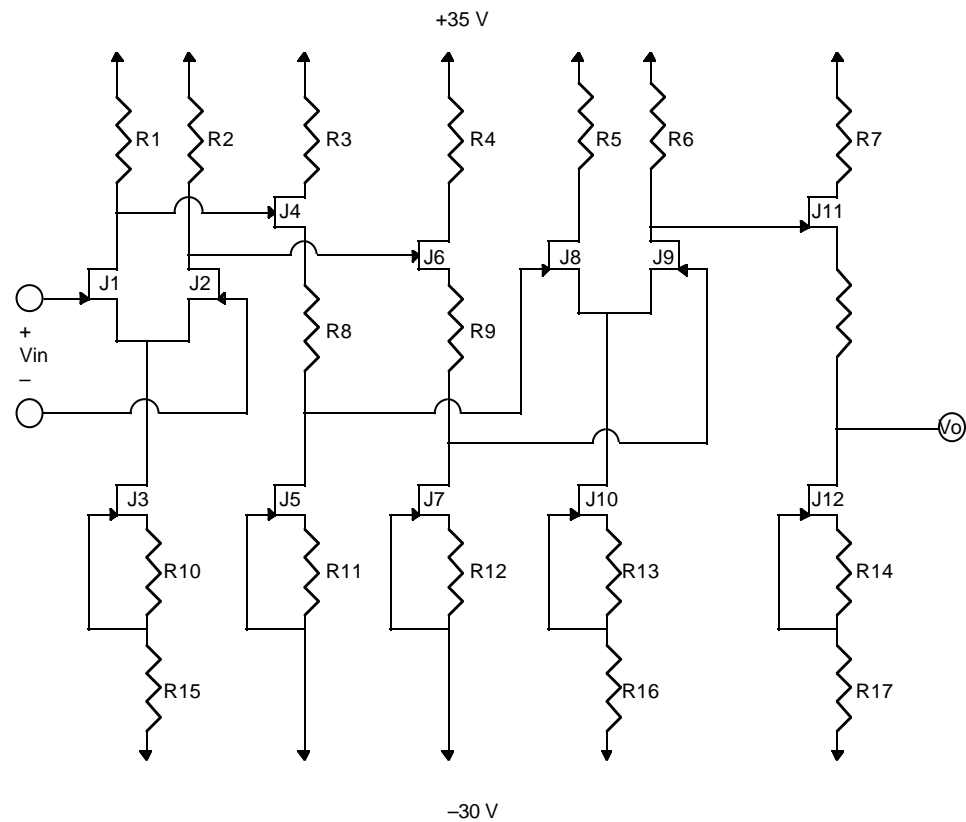


Figure 4. Mask layout.

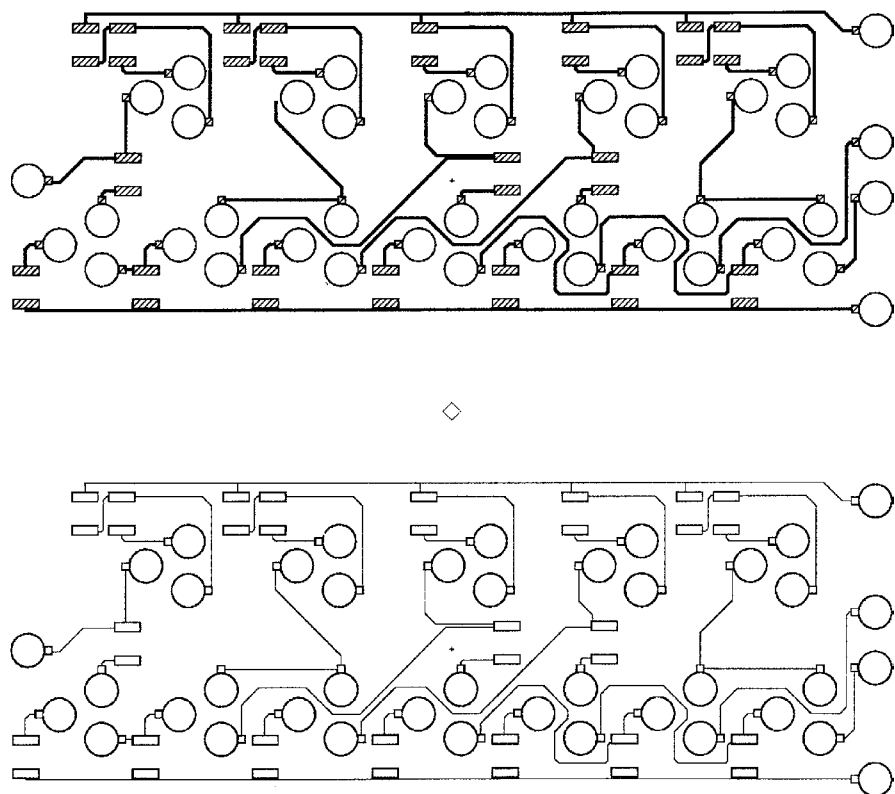


Table 1. Chemical solutions used in PCB fabrication.

Step	Solutions and processing
Nickel and gold etch	400 gm KI potassium iodide 100 gm I ₂ iodine 400 ml H ₂ O etch rate: 400 to 1600 nm/min
Plasma ash	300–400 W, O ₂ for 6–30 min
Piranha clean	100 ml H ₂ SO ₄ 50 ml DI H ₂ O ₂ 15-min dip
Posistrip 830 resist removal	15 min at 90°C
Photoresist (pulled)	KTI 825 Pull rate of 0.43 in./min Thickness 2 µm Exposure time 30 s
Photoresist developer	200 ml Microposit 934 200 ml DI H ₂ O 25 s to develop
Aremco Ceramabond 571 high-temperature epoxy	10 g liquid 15 g powder Air set 4 hr Oven bake 200°F, 4 hr

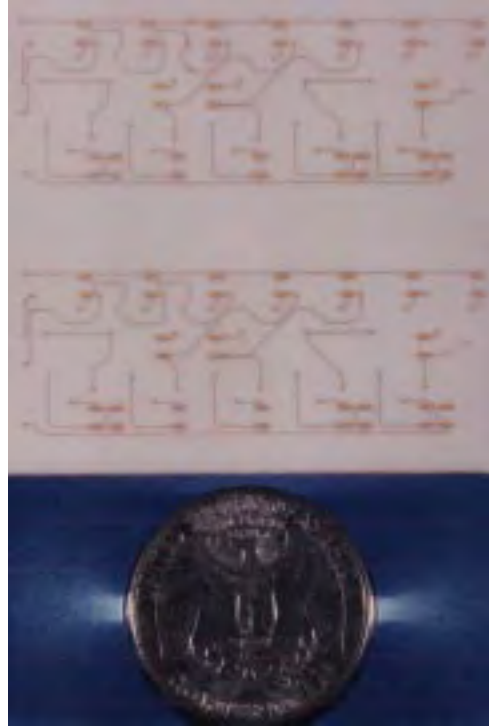
Another cause of the etch-based patterning problem was the presence of a glue layer beneath the gold film on the commercial PCBs. On two of the PCBs, the glue layer contained nickel that was partially etched during the gold-etch step; this caused the gold to lift off from the alumina substrate. To prevent this, we used substrates without the glue layer for subsequent development.

We coated several blank alumina substrates with chrome and gold using an evaporation system to deposit 1 µm of gold (fig. 5). Although the evaporated gold on these PCBs solved the problem caused by the glue layer, it did not withstand the patterning step in the PCB fabrication process and lifted off. Since these PCBs had been drilled to accept the pin receptacles, they were reprocessed with the thick-film gold instead of the thin-film process.

To prepare the substrates for the thick-film coating, we stripped the remaining gold off and cleaned them using a standard piranha cleaning process (table 1). Thick-film paste was then applied to the entire board through an unpatterned 1.1-mil screen and spread across the substrate by a squeegee. We then fired the PCBs at 800°C for 10 min to set the gold paste.

To pattern these devices, a new technique had to be used to apply the photoresist; the holes in the PCB did not allow the usual vacuum-chuck spinner to be used. A pull technique was used to apply an even coat of the resist. A clock motor was used to pull the sample out of a beaker of resist at a rate of 0.43 in./min, giving a 2-µm resist thickness. After the resist was applied to the substrate, the PCB fabrication was then completed by the standard etch process described earlier.

Figure 5. Board after gold patterning.



Several materials were studied for use as bonding agents between the pin receptacles and the alumina PCB. The requirements for bonding these two materials together were very demanding. The bond had to hold the pin receptacles in the alumina while the transistors were being inserted or removed. The process of removing or inserting the transistor put both torsional and linear loads on the adhesive. Once the transistors had been inserted, the adhesive had to withstand 300°C operational temperatures and the thermal stress of heating and cooling. Good electrical contact had to be made between the gold traces and the pin receptacles and maintained throughout the operating regime. Another requirement for the bonding material was that it could not corrode, lift off, or otherwise damage the gold traces.

The first material studied for pin-receptacle bonding was a silver/palladium braze that had been used on other high-temperature test boards. Although the silver/palladium braze provided very good adhesion to the nickel coating on the pin receptacles and good electrical contact to the pin receptacles, it gettered the gold from the alumina PCB at temperatures above 200°C, causing shorts in the circuit.

The second material studied was Loctite Corporation's Ultra Copper™, a silicone-based automotive sealant used in high-temperature (350°C) applications such as exhaust gasketing. This material has a rubbery texture when cured and could not hold the pin receptacles in the board during insertion or removal. It also is not electrically conductive and required some other method for connecting the traces to the pin receptacles.

Two different lead/indium solders were investigated: one that melts at 295°C and one that melts at 300°C. The indium in the solder reduced the gettering of the gold while still maintaining good electrical conductivity, but did not adhere well to the nickel pin receptacles.

A mechanical method for pin receptacle retention was then studied. Small gold “C clips” were obtained that were slightly smaller than the outside diameter of the pin receptacles. The pin receptacles were inserted into the PCB, and the C clips pressed onto the pin receptacles on the back of the PCB. These C clips provided good pull-out strength but little or no torsional strength. To provide the torsional strength, we placed Dupont 5715 gold thick-film conductor around the C clip to anchor it to the pin receptacles. A small amount of the gold conductor was then used to make electrical connection from the pin receptacles to the traces on the front side of the PCB. The gold thick-film paste was applied between the pin receptacles and the gold traces, and the PCB fired at 800°C for 1 min. Although this method did provide good electrical conduction, it had some problems with mechanical strength. Even with the gold thick-film paste, the rotational strength of the joint was not good enough to prevent several of the pin receptacles from rotating during transistor placement, breaking the electrical connection.

The method finally chosen to attach the pin receptacles to the PCBs involved the use of a high-temperature adhesive for the mechanical bond and gold paste for the electrical bond. Aremco Ceramabond 571 adhesive was chosen since it has good adhesion to both the nickel pin receptacles and the alumina substrate. It also has a coefficient of expansion midway between that of alumina and the stainless steel pin receptacles (table 2).

The first part of the process was to make contact to the pin receptacles with a small amount of gold paste. The paste was applied to the trace at the edge of the hole through which the pin receptacles were inserted. When the pin receptacles were pushed through the hole, the lip at the top of the pin receptacles was pushed into the gold paste. Once the pin receptacles were inserted into the hole, the PCB was flipped over and Aremco Ceramabond 571 [6] high-temperature adhesive applied. After a 2-hour air cure and a 2-hour 93°C cure for the adhesive, we fired the PCB at 700°C to activate the gold paste and create the electrical connection between the pin receptacles and the PCB (fig. 6).

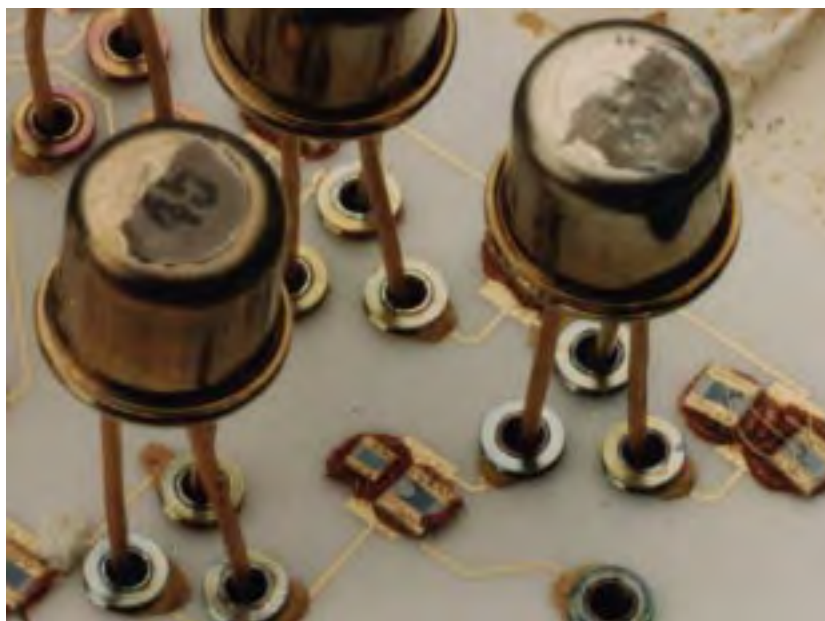
The other major requirement for this PCB was resistor mounting. It was found early in the development of this design that the ruthenium resistors used for hybrid circuits would maintain good tolerance over the entire temperature range. We decided to use available surface mount resistors instead of producing these resistors directly on the PCB.

Since the resistors were surface mounted to the board and not trimmed directly, the following method was used to locate the resistors necessary to meet the required <5-percent tolerance. We chose several values of 5-percent resistors and tested them at both room temperature and at the 300°C operating temperature. Once testing was completed, a computer

Table 2. Aremco high-temperature ceramic adhesive properties.

Characteristic	Value according to product No.			
	503	516	552	571
Major constituent	Alumina	Zirconia	Alumina	Magnesia
Temperature limit				
(°F)	3000	3200	3000	3200
(°C)	1650	1760	1650	1760
No. of components	1	1	1	2
Relative viscosity (CPS)	30–40M	20–30M	37–50M	50–60M
CTE ^a				
(in./°F × 10 ⁻⁶)	4.0	4.1	4.3	7.0
(in./°C × 10 ⁻⁶)	7.2	7.4	7.7	12.6
Volume resistivity				
(W-cm at room temp.—RT)	10 ⁸	10 ⁸	10 ⁸	10 ⁹
(W-cm at 1000°F)	10 ⁵	10 ⁴	10 ⁴	10 ⁵
Thermal conductivity (BTU)	48.8	16.3	49.8	75.6
Dielectric strength				
(V/mil at RT)	253	250	250	255
(V/mil at 1000°F)	240	80	80	100
Torque strength (ft-lb)	5.6	8.6	6.7	22.3
Hardness (Moh's scale)	6	6.5	7	5.5
Porosity (after curing) (%)	<1	<1	<1	<1
Oxidation resistance	Excellent	Excellent	Excellent	Excellent
Alkali resistance	Fair	Excellent	Excellent	Excellent
Acid resistance	Excellent	Good	Good	Fair
Attacked by	HF	HF & H ₂ SO ₄	Concentrated HF	HF
Solvent resistance	Excellent	Excellent	Excellent	Excellent

^aCoefficient of thermal expansion

Figure 6. Closeup of resistor and pin receptacle mounts.

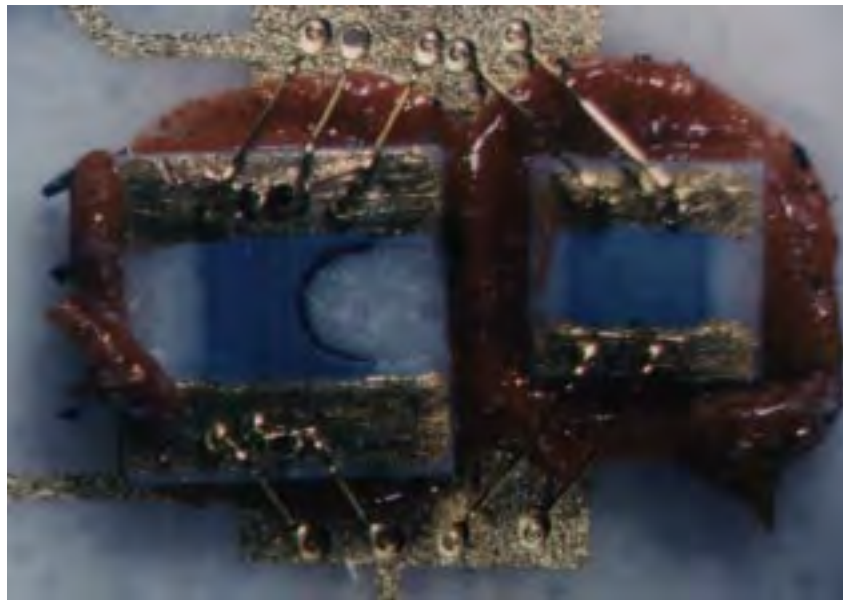
program was written to match these resistors with the required values. This program chose one or two ruthenium resistors for each of the required resistors, and indicated whether the resistors should be wired in parallel or series. In all cases, the values were kept to within 2 percent of the required value at 300°C.

The resistors were attached to the PCB with Ultra Copper™. While allowing a maximum operating temperature of 350°C, Ultra Copper™ also permits the resistors to be easily removed for PCB repair and/or modification. The electrical connections to the resistors were made with 1-mil gold wire bonds. Figure 7 shows a closeup of the resistor bonding technique.

3. Conclusion

Two PCBs have been constructed under this program. The first PCB was used in the construction of the high-temperature radiation-hard amplifier circuit, and the second was kept as a spare. The amplifier PCB has had several transistors inserted and removed through several cycles, with no PCB connection failures to date. At this writing, this PCB has been intermittently operated at temperatures exceeding 300°C for more than 100 hours, with no thermal stress failures of the board.

Figure 7. Closeup of resistor mounting.



Acknowledgments

ARL was supported in this effort by the U.S. Army Space and Strategic Defense Command in Huntsville, Alabama. The authors also wish to thank Charles Scozzie and Jim Blackburn for technical information and support and Tim Mermagen for his help in the layout design process for this board. Finally, the authors would like to thank Jim McGarrity for his support of the SiC program.

References

1. J. Blackburn, C. J. Scozzie, W. Tipton, B. Geil, W. M. DeLancey, J. McGarrity (ARL), and M. Christopher and M. Winland (Physitron), *SiC Junction Field-Effect Transistor Amplifier Operation at 300°C*, Second International High-Temperature Conference (June 1994).
2. J. McGarrity, J. Blackburn, C. J. Scozzie, B. Geil, and W. M. DeLancey, *A SiC JFET Amplifier for Operation in High-Temperature and High Radiation Environments*, to be published in Proc. Space Nuclear Power and Propulsion Conference (January 1995).
3. M. Tomana, R. W. Johnson, R. C. Jaeger, and John Palmour, *A 6H-SiC Hybrid Operational Amplifier for 350°C Operation*, Proc. 42nd Electronic Components and Technology Conference (May 1992).
4. David W. Palmer, *Hybrid Microcircuitry for 300°C Operation*, IEEE Trans. Parts Hybrids Packaging **PHP-13**, No. 3 (September 1977), 252–257.
5. R. Gryzbowski, *Development of 600°C Device Test Fixture*, Proc. 1st Int. High-Temperature Electronics Conference (June 1991).
6. Aremco Products, Inc., *High-Temperature Ceramic Adhesives*, Bulletin No. M2 (April 1994).

Distribution

Admnstr
Defns Techl Info Ctr
Attn DTIC-OCP
8725 John J Kingman Rd Ste 0944
FT Belvoir VA 22060-6218

Defns Special Weapons Agency
Attn RAES L Cohn
Attn RAES L J Palkuti
6801 Telegraph Rd
Alexandria VA 22310-3398

US ARDEC
Attn AMSTA-AR-AEF-A R Goodman
Adelphi MD 20783-1197

Hdqtrs Dept of the Army
Attn DAMO-FDQ MAJ M McGonagle
Attn DAMO-FDQ D Schmidt
400 Army Pentagon
Washington DC 20310-0460

US Army Sp & Strtgc Defns Cmnd
Attn CSSD-SD-A A Kuehl
Attn CSSD-SD-AM A Corder
Attn CSSD-SD-AM C Harper
Attn CSSD-SD-AM G Little
Attn CSSD-SD-AM K Blankenship
Attn CSSD-SD-AM P Adams
Attn CSSD-SD-AM R Goodman
Attn CSSD-SD-EV R Bradshaw
Attn CSSD-SL-S I Merritt
PO Box 1500
Huntsville AL 35807-3801

US Army Special Oprn Cmnd
Attn A Gies
Attn DCS-FCI-CD-TB S Raineri
Attn E Blough Bldg D3206 Rm 503
FT Bragg NC 28307-5200

US Army TECOM
Attn STEWS-NE J Meason
White Sands Missile Range NM 88002

USACOE
Attn CEHND-SY J Loyd
Attn CEHND-SY R Johnson
PO Box 1600
Huntsville AL 35807-4301

Nav Rsrch Lab
Attn C Dozier
Attn Code 6816 W C Jenkins
Attn Code 8120 A Fox
4555 Overlook Ave SW
Washington DC 20375

Nav Rsrch Lab
Attn Code 2620 Techl Lib
Washington DC 20375

Nav Surface Warfare Ctr
Attn Code WA50
Attn Code WA501 Nav Nuc Programs Ofc
Attn Code WA52
Attn Code E-42 Techl Lib
White Oak MD 20910

Nav Surface Weapons Ctr
Attn Code WR Rsrch & Technology Dept
Attn DX-21 Library Div
Dahlgren VA 22448

Nav Weapons Spprt Ctr
Attn Code 6054 T Turflinger
Bldg 2506
Crane IN 47522

USAF Sp & Mis Sys Ctr
Attn K Basany/MBSPH
2400 E El Segundo Blvd PO Box 92960
Los Angeles CA 90009-2960

Physitron
Attn G Grant
Attn J Sheehy
Attn M Christopher
Attn T Henderson
3304 Westmill Dr
Huntsville AL 35805

Distribution

Physitron Inc
Attn J Azarewicz
Attn M Rose
11545 W Bernardo Ct Ste 205
San Diego CA 92128-0950

US Army Rsrch Lab
Attn AMSRL-MA L W Johnson
Watertown MA 02172-0001

US Army Rsrch Lab
Attn AMSRL-WT-PC A Barrows
Aberdeen Proving Ground MD 21005-5066

US Army Rsrch Lab
Attn AMSRL-BE COL R Evans
Attn AMSRL-BE-A D R Veaszey
Attn AMSRL-SL J Wade
White Sands Missile Range NM 88002-5513

US Army Rsrch Lab
Attn AMSRL-PS-P J M McGarrity
FT Monmouth NJ 07703

US Army Rsrch Lab
Attn AMSRL-WT D Eccleshall
Attn AMSRL-WT G Klem
Attn AMSRL-WT-NC R Lottero
Attn AMSRL-WT I May
Attn AMSRL-WT-T W F Morrison
Attn AMSRL-CI W H Mermagen Sr
Attn AMSRL-HR R L Keesee
Attn AMSRL-WT-W C Murphy
Attn AMSRL-WT-W L Puckett
Attn AMSRL-WT-WB W P D'Amico
Attn AMSRL-WT-WD A Niiler
Attn AMSRL-SL-CS J McCullen
Attn AMSRL-OP-AP-L Techl Lib
(3 copies)
Attn AMSRL-HR-SD T Mermagen
Aberdeen Proving Ground MD 21005-5000

US Amy Rsrch Lab
Attn AMSRL-WT-TB L Ferguson
Aberdeen Proving Ground MD 21010-5423

US Army Rsrch Lab
Attn AMSRL-SL-CO A Bevec
Attn AMSRL-SL-CO D Davis
Attn AMSRL-SL-CO G W Still
Attn AMSRL-SL-CS D Manyak
Attn AMSRL-SL-CE Dr Beilfuss
Attn AMSRL-SL-CS M Bumbaugh
Attn AMSRL-SL-CS T Flory
Edgewood MD 21010-5423

US Army Rsrch Lab
Attn AMSRL-VS W Elber
Hampton VA 23681-0001

US Army Rsrch Lab
Attn AMSRL-VP R Bill
21000 Brookpark Rd
Cleveland OH 44135-3191

US Army Rsrch Lab
Attn AMSRL-BE-SA D Snider
Attn AMSRL-CI-LL Tech Lib (3 copies)
Attn AMSRL-CP-CC J Predham
Attn AMSRL-CS-AL-TA Mail & Records
Mgmt
Attn AMSRL-CS-AL-TP Techl Pub (3 copies)
Attn AMSRL-IS P Emmerman
Attn AMSRL-LT R Weinraub
Attn AMSRL-PP B Fonoroff
Attn AMSRL-SE-DE J Miletta
Attn AMSRL-SE-DP A Stewart
Attn AMSRL-SE-DP R A Kehs
Attn AMSRL-SE-DS C Fazi
Attn AMSRL-SE-DS S Sadow
Attn AMSRL-SE-DT L Jasper
Attn AMSRL-SE-E J Pellegrino
Attn AMSRL-SE-EO N Gupta
Attn AMSRL-SE-EO T Tayag
Attn AMSRL-SE-EP J Corrigan
Attn AMSRL-SE-EP S Karamchetty
Attn AMSRL-SE-DP G Huttlin
Attn AMSRL-SE-EM G Simonis
Attn AMSRL-SE-EP A Lelis
Attn AMSRL-SE-EP B McLean

Distribution

US Army Rsrch Lab (cont'd)

Attn AMSRL-SE-EP C Scozzie

(10 copies)

Attn AMSRL-SE-EP D Robertson

Attn AMSRL-SE-EP E Boesch

Attn AMSRL-SE-EP G Ovrebo

Attn AMSRL-SE-EP J Benedetto

Attn AMSRL-SE-EP K Bennett

Attn AMSRL-SE-EP M Delancey

(10 copies)

Attn AMSRL-SE-EP T Oldham

Attn AMSRL-SE-EP T Taylor

Attn AMSRL-SE-EP W Tipton

US Army Rsrch Lab (cont'd)

Attn AMSRL-SE-DP D Conrad

Attn AMSRL-SE-ES M Patterson

Attn AMSRL-SE-IS V DeMonte

Attn AMSRL-SE-PC A Goldberg

Attn AMSRL-SE-RL B Reams

Attn AMSRL-SE-RL B Rod

Attn AMSRL-SE-RL R Zeto

Attn AMSRL-SE-RL T Griffin

Attn AMSRL-SE-RL B Geil (15 copies)

Attn AMSRL-SE-SA H Brann

Attn AMSRL-WT M Abe

Adelphi MD 20783-1197

REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188	
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.				
1. AGENCY USE ONLY (Leave blank)		2. REPORT DATE November 1996		3. REPORT TYPE AND DATES COVERED Final, from January 1994 to January 1995
4. TITLE AND SUBTITLE A High-Temperature Printed Circuit Board			5. FUNDING NUMBERS PE: 612120	
6. AUTHOR(S) Bruce R. Geil and Merle W. DeLancey				
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) U.S. Army Research Laboratory Attn: AMSRL-SE-RL 2800 Powder Mill Road Adelphi, MD 20783-1197			8. PERFORMING ORGANIZATION REPORT NUMBER ARL-MR-339	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) U.S. Army Space and Strategic Defense Command PO Box 1500 Huntsville, AL 35807-3801			10. SPONSORING/MONITORING AGENCY REPORT NUMBER	
11. SUPPLEMENTARY NOTES AMS code: 612120.H2500 ARL PR: 425323				
12a. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution unlimited.			12b. DISTRIBUTION CODE	
13. ABSTRACT (Maximum 200 words) Working with the U.S. Army Space and Strategic Defense Command, the Army Research Laboratory has developed an easy-to-produce, reliable, high-temperature printed circuit board for radiation studies of circuits that use silicon carbide transistors. This board is designed to operate at temperatures beyond 300°C. The board consists of an alumina substrate with thick-film gold traces. Stainless-steel pin receptacles are used to mount the transistors, allowing easy insertion and removal. Ruthenium oxide resistors are glued to the substrate and wire-bonded for electrical connection.				
14. SUBJECT TERMS Silicon carbide, packaging			15. NUMBER OF PAGES 19	
			16. PRICE CODE	
17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT UL	

DEPARTMENT OF THE ARMY
U.S. Army Research Laboratory
2800 Powder Mill Road
Adelphi, MD 20783-1197

An Equal Opportunity Employer